

REMARKS

2 Claims 51-77 are pending in the present application. Claims 51-61
3 stand rejected under 35 U.S.C. §103(a) for obviousness over U.S. Patent
4 No. 5,672,525 to Pan (the Pan '525 patent) in combination with U.S.
5 Patent No. 5,705,409 to Witek (the Witek patent) and U.S. Patent
6 No. 5,750,435 to Pan (the Pan '435 patent). Claims 51-75 stand
7 revisionally rejected under the judicially-created doctrine of obviousness-
8 type double patenting over claims 22-30 of co-pending application
9 number 08/993,663.

10 Applicants traverse the rejections and urge allowance of the
11 present application.

12 Referring to the 35 U.S.C. §103 rejections, the teachings of the
13 references do not support an obviousness rejection of the claims. An
14 obviousness rejection requires consideration of all the elements of the
15 claimed invention. Further, all such elements must be shown to be
16 suggested by the prior art when making a rejection based upon
17 obviousness under 35 U.S.C. §103(a). *In re Fine*, 837 F.2d 1071, 5
18 USPQ2d 1596 (Fed. Cir. 1987).

19 Independent claim 51 defines a method of forming a transistor
20 gate comprising, in part, providing at least one of fluorine or chlorine
21 within a gate oxide layer and forming a gate proximate the gate oxide
22 layer after the providing. The subject matter of claim 51 is not shown
23 or suggested in the prior art of record.

1 None of the prior art references, taken alone or in combination,
2 teach or suggest providing at least one of fluorine and chlorine within
3 a gate oxide layer, and forming a gate proximate the gate oxide layer
4 *after the providing* as claimed.

5 Referring initially to the Pan '525 patent, such clearly discloses
6 with reference to Figs. 1C-1E the formation of the gate prior to
7 fluorination of layer 18. Referring to the Pan '435 patent, such clearly
8 discloses in Figs. 1A-1B the formation of gate electrode 16 and
9 subsequent implantation of fluorine ions in Fig. 1B following the
10 formation of gate electrode 16. Referring to Fig. 8 and Fig. 9 of the
11 Witek patent, such fails to teach or suggest the formation of a gate
12 oxide layer over a semiconductive substrate in combination with forming
13 a gate proximate the gate oxide layer after the providing as claimed.

14 Accordingly, the teachings of the Pan '525 patent, the Pan '435
15 patent and the Witek patent, taken singularly or in combination, fail to
16 teach or suggest limitations of claim 51. As not one of the cited
17 references discloses such recited limitations, it is inconceivable that the
18 references could, singularly or in any combination, suggest such recited
19 limitation. Claim 51 defines patentable subject matter over the prior
20 art of record.

21 Claims 52-54 and claims 76-77 depend from independent claim 51
22 and therefore are in condition for allowance for the reasons discussed
23 above with respect to claim 51 as well as for their own respective
24 features which are neither shown nor suggested by the cited art.

1 Referring to independent claim 55, a method of forming a
2 transistor gate is defined comprising, in part, forming a gate and a gate
3 oxide layer in overlapping relation, the gate oxide layer having a center
4 and outwardly exposed opposing edges laterally aligned with the edges
5 of the gate; and concentrating at least one of chlorine or fluorine in
6 the gate oxide layer having the outwardly exposed opposing edges and
7 within the overlap. The subject matter of independent claim 55 is not
8 shown or suggested in the prior art of record.

9 None of the prior art references, taken alone or in combination,
10 teach or suggest forming a gate oxide layer having a center and
11 outwardly exposed opposing edges laterally aligned with the edges of the
12 gate, and concentrating at least one of chlorine or fluorine in the gate
13 oxide layer *having the outwardly exposed opposing edges* as claimed.

14 Referring initially to the Pan '525 patent, the structure of
15 Figs. 1A-1J and Figs. 2-5 fails to teach or suggest the gate oxide having
16 a center and outwardly exposed opposing edges laterally aligned with the
17 edges of the gate and concentrating at least one of chlorine or fluorine
18 in the gate oxide layer having the outwardly exposed opposing edges.
19 As described in col. 5, lines 6-8, of the Pan '525 patent, the structure
20 of Fig. 1C further receives a blanket thin silicon oxide dielectric
21 layer 18 to provide the structure of Fig. 1D. Fluorination thereafter
22 occurs with respect to Fig. 1E. Accordingly, the Pan '525 patent fails
23 to teach or suggest concentrating at least one of chlorine or fluorine in
24

1 the gate oxide layer having the outwardly exposed opposing edges as
2 claimed.

3 Further, the Pan '435 patent fails to teach or suggest the
4 formation of the gate oxide layer having a center and outwardly exposed
5 opposing edges laterally aligned with the edges of the gate. Referring
6 to Figs. 1A-1E of the Pan '435 patent, all such disclosed structures
7 additionally fail to teach or suggest concentrating at least one of
8 chlorine or fluorine in the gate oxide layer having the outwardly exposed
9 opposing edges as claimed.

10 In addition, the disclosed structures of the Witek patent fail to
11 teach or suggest the formation of the gate and the gate oxide layer as
12 claimed having outwardly exposed opposing edges laterally aligned with
13 the edges of the gate and concentrating at least one of chlorine or
14 fluorine in the gate oxide layer having the outwardly exposed opposing
15 edges.

16 Accordingly, the teachings of the Pan '525 patent, the Pan '435
17 patent and the Witek patent, taken alone or in combination, fail to
18 teach or suggest positively-defined limitations of independent claim 55.
19 Accordingly, claim 55 is patentable over the prior art of record.

20 Claims 56-61 depend from independent claim 55 and therefore are
21 in condition for allowance for the reasons discussed above with respect
22 to claim 55 as well as for their own respective features which are
23 neither shown nor suggested by the cited art.

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With regards to the double patenting rejection, application serial number 08/993,663 has been abandoned by Applicants and the claims thereof are currently being prosecuted in application serial number 09/332,255. Accordingly, it is believed that the obviousness-type double patenting rejection is improper in view of the abandonment of application serial number 08/993,663.

14 || Applicants respectfully request allowance of all pending claims.

15 The Examiner is requested to phone the undersigned if the
16 Examiner believes such would facilitate prosecution of the present
17 application. The undersigned is available for telephone consultation at
18 any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

22 Dated: 2/9/00

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